**AMENDMENTS TO THE SPECIFICATION:**

Please replace paragraph 0022 with the following amended paragraph.

Next, in step 104 the surface of the substrate is selectively etched using a combination of suitable isotropic and anisotropic etches to recess exposed portions of the semiconductor substrate surface, i.e., in areas not protected by gate electrodes and adjacent spacers, below the level of interface between the gate dielectric and the substrate under the gate. Thus, preferably, the sub etch forms recesses from [[form]] 30Å to about 700Å below the original surface level and most preferably, 30 to about 300Å. Once recessed, the semiconductor substrate surface can be optionally undercut with a semiconductor etch to provide a small overlap between the gate electrode edges and the etched substrate surface (preferably, 10Å-30Å of overlap). Then, in step 106 a thin semiconductor layer (<100Å) adjacent to the recessed semiconductor surface is doped using known doping techniques (e.g. gas phase doping) to laterally form thin (<100Å) doped extensions which overlap gate electrode edges by 10-30Å. Alternatively, a thin epi layer is selectively deposited and doped, preferably, with in situ doping to laterally form thin (<100Å) doped extensions which overlap gate electrode edges by 10Å-30Å. In particular, the doped lateral extension layer should be made substantially thicker than the depletion width of the silicide-semiconductor Schottky diode (a typical depletion width of such diode is about 10Å) in order to reduce the contact resistance to an acceptable level. Accordingly, a preferred thickness range of doped laterally thin extension is from about 10Å to about 100Å.